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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,443	03/30/2004	Hirofumi Harada	S004-5253	3384

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EXAMINER	
TOLEDO, FERNANDO L	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,443	HARADA, HIROFUMI	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 8-18* is/are pending in the application.

4a) Of the above claim(s) *8-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 3 April 2003. It is noted, however, that applicant has not filed a certified copy of the 2003-099926 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Hshieh (US 2003/0089946 A1).

4. In re claim 1, Hshieh, in the United States Patent Application Publication US 2003/0089946 A1; figures 1 – 12C discloses, implanting an impurity of a second conductivity type 204 into the main surface of the semiconductor substrate of the first conductivity type and thermally diffusing the impurity of the second conductivity type to form a body region of the second conductivity type; carrying out an anisotropic etching (Figure 8A) on a region of the main surface of a semiconductor substrate to form a trench 206 having several wall surfaces;

forming a gate oxide film 210t and 210d over the main surface of the semiconductor substrate and along the wall surface of the trench (Figure 8B); depositing a polycrystalline silicon layer 211g into the trench and over the main surface of the semiconductor (¶0050) so as to overlie the gate oxide film; etching the polycrystalline silicon layer so as to remove the polycrystalline silicon layer overlying the main surface of the semiconductor substrate and so as to remove the polycrystalline silicon layer within the trench to a predetermined depth from the main surface of the semiconductor substrate to form a gate electrode within the trench (Figure 8F and ¶0050); implanting an impurity of the first conductivity type into the main surface of the semiconductor substrate to form a source region 212 of the first conductivity type; implanting an impurity of the second conductivity type 215 into the main surface of the semiconductor substrate to form a body contact region of the second conductivity type; depositing an intermediate insulating film 216 over the main surface of the semiconductor substrate and the gate electrode; etching back the intermediate insulating film overlaying the main surface of the semiconductor substrate so as to entirely expose the source region and the body contact region forming the main surface of the semiconductor substrate (Figure 8G); and forming a source metal electrode 218 over the main surface of the semiconductor substrate.

5. In re claim 14, Hshieh discloses wherein the etching back step includes the step of etching back the intermediate insulating film to planarized the main surface of the semiconductor substrate; and wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure (¶0052 and Figure 8G).

6. In re claim 15, Hshieh discloses wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure over the main surface of the semiconductor substrate (Figure 8G).

7. In re claim 16, Hshieh discloses wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure so as to cover the entire main surface of the semiconductor substrate (Figure 8G).

8. In re claim 17, Hshieh discloses wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure so as to increase a contact area between the source metal electrode and the source and body contact regions to thereby substantially reduce a resistance between (Figure 8G).

9. In re claim 18, Hshieh discloses wherein the etching back step includes the step of etching back the intermediate insulating film so as to planarize the main surface of the semiconductor substrate to facilitate the formation of the source metal electrode as a planar structure over the main surface of the semiconductor substrate (Figure 8G).

Response to Arguments

10. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

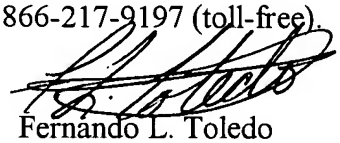
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Fri 12pm-7:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Fernando L. Toledo
Patent Examiner
Art Unit 2823

flt
27 April 2006